1. A/D Conversion Overview
2. Optimizing Data Converter Interfaces
3. DACs and DDSs
A Sampled Data System

AMPLITUDE QUANTIZATION

DISCRETE TIME SAMPLING

\[ f_s = \frac{1}{t_s} \]
Fundamental Dimensions of Data Converter Performance

- Sampling/Update Rate (Nyquist Constraint)
- Resolution (Dynamic Range between “Clipping Ceiling” and “Quantization Floor”)
- Accuracy and Linearity
- Power consumption
Converters work across domains

- Transfer Function: Signal Out vs. Signal In (crossplot)
- Continuous time domain, analog (oscilloscope)
- Continuous frequency domain, analog (spectrum analyzer)
- Discrete time, analog (switched capacitor, z-domain)
- Discrete time, digital, time domain (sequence of bytes)
- Discrete time, digital, frequency domain (FFT output)
- “Real” signals vs. complex (or quadrature) signals
Transfer Function for Ideal 3-bit Unipolar ADC

ANALOG INPUT

DIGITAL OUTPUT (STRAIGHT BINARY)

000
001
010
011
100
101
110
111

1/8 1/4 3/8 1/2 5/8 3/4 7/8 FS

1 LSB
1/2 LSB
1 LSB
1/2 LSB
Quantization: 
The Size of a Least Significant Bit (LSB)

<table>
<thead>
<tr>
<th>RESOLUTION N</th>
<th>$2^N$</th>
<th>VOLTAGE (10V FS)</th>
<th>ppm FS</th>
<th>% FS</th>
<th>dB FS</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-bit</td>
<td>4</td>
<td>2.5 V</td>
<td>250,000</td>
<td>25</td>
<td>– 12</td>
</tr>
<tr>
<td>4-bit</td>
<td>16</td>
<td>625 mV</td>
<td>62,500</td>
<td>6.25</td>
<td>– 24</td>
</tr>
<tr>
<td>6-bit</td>
<td>64</td>
<td>156 mV</td>
<td>15,625</td>
<td>1.56</td>
<td>– 36</td>
</tr>
<tr>
<td>8-bit</td>
<td>256</td>
<td>39.1 mV</td>
<td>3,906</td>
<td>0.39</td>
<td>– 48</td>
</tr>
<tr>
<td>10-bit</td>
<td>1,024</td>
<td>9.77 mV (10 mV)</td>
<td>977</td>
<td>0.098</td>
<td>– 60</td>
</tr>
<tr>
<td>12-bit</td>
<td>4,096</td>
<td>2.44 mV</td>
<td>244</td>
<td>0.024</td>
<td>– 72</td>
</tr>
<tr>
<td>14-bit</td>
<td>16,384</td>
<td>610 μV</td>
<td>61</td>
<td>0.0061</td>
<td>– 84</td>
</tr>
<tr>
<td>16-bit</td>
<td>65,536</td>
<td>153 μV</td>
<td>15</td>
<td>0.0015</td>
<td>– 96</td>
</tr>
<tr>
<td>18-bit</td>
<td>262,144</td>
<td>38 μV</td>
<td>4</td>
<td>0.0004</td>
<td>– 108</td>
</tr>
<tr>
<td>20-bit</td>
<td>1,048,576</td>
<td>9.54 μV (10 μV)</td>
<td>1</td>
<td>0.0001</td>
<td>– 120</td>
</tr>
<tr>
<td>22-bit</td>
<td>4,194,304</td>
<td>2.38 μV</td>
<td>0.24</td>
<td>0.000024</td>
<td>– 132</td>
</tr>
<tr>
<td>24-bit</td>
<td>16,777,216</td>
<td>596 nV*</td>
<td>0.06</td>
<td>0.000006</td>
<td>– 144</td>
</tr>
</tbody>
</table>

*600nV is the Johnson Noise in a 10kHz BW of a 2.2kΩ Resistor @ 25°C
Remember: 10-bits and 10V FS yields an LSB of 10mV, 1000ppm, or 0.1%.
All other values may be calculated by powers of 2.
Nyquist Analog to Digital Converters:

- **Fs/2**
- **Fs**
- **Fb**
- **Fs - Fb**
- **2Fs**
- **Fs + Fb**
- **2Fs - Fb**

**Aliasing**

**Antialiasing Filter**

Freq

Fb

Fs/2

Fs

Fb

Fs - Fb

Fs

Fs + Fb

2Fs - Fb

2Fs

2Fs
Data Converter Selection: It's Not Just Bits and Speed

- Making tradeoffs involves many variables
- AC and DC performance
- Power consumption
- Degree of integration
- Ease of use
  - Output data formatting
  - Supply voltages
  - Package size
  - Integrated Functionality
- Cost
- Reputation of IC vendor
  - Design Tools (Simulation, Evaluation kits)
  - Applications expertise
  - Clear, concise documentation
  - Help with product selection
The Comparator: A 1-Bit ADC

Differential Analog Input

Comparator Output

LOGIC OUTPUT

LATCH ENABLE

Comparator

V_HYSTERESIS

"0"

"1"

0

Differential Analog Input
ADC Architectures, Applications, Resolution, Sampling Rates

- **INDUSTRIAL MEASUREMENT**
- **VOICEBAND, AUDIO, Industrial**
- **DATA ACQUISITION**
- **VIDEO, IF SAMPLING, SOFTWARE RADIO, ETC.**

**RESOLUTION (BITS)**

**SAMPLING RATE (Hz)**

- **CURRENT STATE-OF-THE-ART (APPROXIMATE)**
- **PIPELINE**

- **Σ-Δ**

1. ADC Architectures, Applications, Resolution, Sampling Rates
2. Table or list of sampling rates and resolutions.
3. Diagram showing the relationship between resolution and sampling rate for different applications.
5. Applications such as industrial measurement, voiceband, audio, and data acquisition.
Successive Approximation ADCs (SAR)
Typical Muxed Data Acquisition System
Basic Successive Approximation ADC (Feedback Subtraction ADC)
3-Bit Switched Capacitor DAC

SWITCHES SHOWN IN TRACK (SAMPLE) MODE
Successive Approximation ADC Algorithm

ASSUME X = 45

IS X \geq 32 ?

YES \rightarrow RETAIN 32 \rightarrow 1

IS X \geq (32 + 16) ?

NO \rightarrow REJECT 16 \rightarrow 0

IS X \geq (32 + 8) ?

YES \rightarrow RETAIN 8 \rightarrow 1

IS X \geq (32 + 8 + 4) ?

YES \rightarrow RETAIN 4 \rightarrow 1

IS X \geq (32 + 8 + 4 + 2) ?

NO \rightarrow REJECT 2 \rightarrow 0

IS X \geq (32 + 8 + 4 + 2 + 1) ?

YES \rightarrow RETAIN 1 \rightarrow 1

X = 32 + 8 + 4 + 1 = 45_{10} = 101101_{2}

TOTALS:
Typical SAR ADC Timing

- **SAMPLE X**
  - **CONVST**
  - **CONVERSION TIME**
  - **EOC, BUSY**
  - **OUTPUT DATA**

- **SAMPLE X+1**
  - **CONVST**
  - **CONVERSION TIME**
  - **TRACK/ACQUIRE**
  - **DATA X**

- **SAMPLE X+2**
  - **CONVST**
  - **CONVERSION TIME**
  - **TRACK/ACQUIRE**
  - **DATA X+1**
AD7982 18-Bit, 2 MSPS 15mW PulSAR® ADC
AD7609 8-Channel Differential DAS with 18-Bit Bipolar Simultaneous 200KSPS Sampling ADC

Input protection
ADC Architectures, Applications, Resolution, Sampling Rates ($\Sigma-\Delta$)

- **INDUSTRIAL MEASUREMENT**
- **VOICEBAND, AUDIO, SDR**
- **DATA ACQUISITION**
- **VIDEO, IF SAMPLING, SOFTWARE RADIO, ETC.**

### SAMPLING RATE (Hz)

- 10
- 100
- 1k
- 10k
- 100k
- 1M
- 10M
- 100M
- 1G

### RESOLUTION (BITS)

- 24
- 22
- 20
- 18
- 16
- 14
- 12
- 10
- 8

**CURRENT STATE-OF-THE-ART (APPROXIMATE)**
First-Order Sigma-Delta ADC

\[ V_{IN} \rightarrow + \rightarrow \sum \rightarrow - \rightarrow \int \rightarrow + \rightarrow A \rightarrow + \rightarrow - \rightarrow \text{CLOCK} \rightarrow Kf_s \rightarrow \text{DIGITAL FILTER AND DECIMATOR (n order CIC)} \rightarrow \text{N-BITS} \]

\[ \sum \rightarrow +V_{REF} \rightarrow \text{LATCHED COMPARATOR (1-BIT ADC)} \rightarrow -V_{REF} \rightarrow 1\text{-BIT DATA STREAM} \rightarrow 1\text{-BIT DAC} \rightarrow 1\text{-BIT, } Kf_s \]

\[ \text{SIGMA-DELTA MODULATOR} \]
Oversampling, Digital Filtering, Noise Shaping, and Decimation

A

\[ f_s \]

\[ \text{ADC} \]

\[ \downarrow f_s \]

\[ \downarrow Kf_s \]

\[ \downarrow f_s \]

\[ \downarrow Kf_s \]

\[ \downarrow f_s \]

\[ \Sigma \Delta \text{MOD} \]

\[ \rightarrow \text{DIGITAL FILTER} \]

\[ \rightarrow \text{DEC} \]

Nyquist Operation

B

C

QUANTIZATION

\[ \text{NOISE} = q / 12 \]

\[ q = 1 \text{ LSB} \]

DIGITAL FILTER

REMOVED NOISE

REMOVED NOISE

\[ f_s \]

\[ 2 \]

\[ Kf_s \]

\[ 2 \]

\[ f_s \]

\[ 2 \]

\[ Kf_s \]

\[ 2 \]
Replacing Integrators with Resonators Gives a Bandpass Sigma-Delta ADC

\[\sum H(f)\]

DAC

Digital BPF Filter & Decimator

Clock \(K \times Fs\)

\(A_{in}\)

\(F_s\)

\(F_c\)

Digital BPF Filter Response

Shaped Quantization Noise

\(BW < 2 \times Fs\)
AD9262 16-Bit, 2.5/5/10MHz, 30-160MSPS
Dual Continuous Time \(\Sigma\Delta\) ADC

**KEY FEATURES**

- SNR: 85 dBFS to 10 MHz input
- SFDR: 87 dBc to 10 MHz input
- Noise Figure: 15dB
- Power: 675 mW
- Sample rate converter: 30-160 MSPS
- Selectable bandwidth:
  - 5/10/20MHz complex
- Passive input network
  - No ADC driver amplifier required
- Alias immune
  - No Anti-Alias Filter
- Integrated Functions:
  - Decimation filter and Sample Rate Conv.
  - Quadrature Error and DC offset correction
  - PLL clock multiplier
  - Low drift voltage reference
- Serial Control Interface
- 1.8 V Analog supply

**Temp**

-40°C – +85°C

**Package**

9 x 9 mm LFCSP Pb-Free

**Sampling**

Now

**Final Release**

In Production
ADC Architectures, Applications, Resolution, Sampling Rates

- **SAR**: Industrial Measurement
- **Σ-Δ**: Voiceband, Audio, SDR
- **Data Acquisition**: Video, IF Sampling, Software Radio, etc.
- **Pipeline**: Current State-of-the-Art (Approximate)
3-bit All-Parallel (Flash) Converter

A KEY BUILDING BLOCK FOR PIPELINED ADCs
6-bit Two-Stage Subranging ADC

Residue Waveforms at Input of N2 SADC

(A) IDEAL N1 SADC

(B) NONLINEAR N1 SADC

R = RANGE OF N2 SADC

MISSING CODES

X

Y

MISSING CODES
6-Bit Subranging Error Corrected ADC
N1 = 3, N2 = 4

OFFSET
ANALOG INPUT

SAMPLE AND HOLD

N1 3-BIT SADC
N1 3-BIT SDAC

ADDER (+ 001)

OVERRANGE LOGIC AND OUTPUT REGISTER

DATA OUTPUT

OFFSET
MSB
CARRY

RESIDUE SIGNAL

Generalized Pipeline Stages in a Subranging ADC with Error Correction
Clock Issues in Pipelined ADCs

![Diagram of a pipelined ADC with clock issues]

- **V\textsubscript{IN}**
- **INPUT T/H**
- **STAGE 1 T/H**
- **STAGE 2 T/H**
- **STAGE 3 T/H**
- **FLASH**
- **CLOCK**
- **DATA OUT**

**PIPELINE DELAY**
Typical Pipelined ADC Timing for AD9629 12-Bit, 80-MSPS ADC

PIPELINE DELAY (LATENCY) = 8 CLOCK CYCLES
AD9629 12-bit 20-80MSPS Pipeline ADC (1.8V 100mW @ 80MSPS)
Summary: SAR vs. Pipelined ADCs

**SAR ADCs**
- Resolution to 18 to 24 bits
- Sample Rates to 10 MSPS @ 16 bits
- Excellent DC Specifications
- Single-Shot Operation
- No Minimum Sample Rate
- No Latency (Pipeline Delay)
- Ideal for Muxed Applications
- Complete AC Specifications
- Easy to Use
- Key Applications:
  - Data Acquisition
  - Instrumentation
  - Industrial Process Control
  - Spectral Analysis
  - Medical Imaging (Xray)
  - ATE

**PIPELINED ADCs**
- Resolution to 16 bits
- Sample Rates to 1000MSPS+
- More Emphasis on AC Specifications
- Must Sample Continuously
- Minimum Sample Rate Specified
- Pipeline Delay
- Not Suitable for Muxed Systems
- Complete AC Specifications
- Easy to Use
- Key Applications
  - Digital or Software Radio Receivers
  - Spectral Analysis
  - Medical Imaging
  - Display Electronics
  - Radar
## Relative comparison of ADC Architecture

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Relative Conversion Time</th>
<th>Relative Power &amp; HW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash</td>
<td>1</td>
<td>$2^N$</td>
</tr>
<tr>
<td>Folding</td>
<td>1</td>
<td>$&lt;2^N$</td>
</tr>
<tr>
<td>Multi-step</td>
<td>~2</td>
<td>$M*2^{N/M}$</td>
</tr>
<tr>
<td>Pipelined (2-stage)</td>
<td>~2</td>
<td>~N</td>
</tr>
<tr>
<td>Algorithmic</td>
<td>~2N</td>
<td>1</td>
</tr>
<tr>
<td>SAR</td>
<td>~2N</td>
<td>~N</td>
</tr>
<tr>
<td>Integrating</td>
<td>$2^N$</td>
<td>~1</td>
</tr>
</tbody>
</table>
Interleaved Parallel ADC
Parallel ADC
Dynamic Performance

• Parallel ADC architecture is limited to 8 to 10-bit dynamic performance

• Quantifiable errors are coming from:
  • Gain mismatch;
  • Imperfect phasing between A/D converters;
  • Offset mismatch.

• These errors produce spectral distortion such as:
  • Alias spurs for the gain and timing differences;
  • Spur located at Nyquist rate for the Offset mismatch.
AD9286: 8-bit 500MSPS Interleaved ADC
Single-Ended DC Coupled Amplifier Drivers for ADCs
Op Amp Gain and Level Shifting Circuits

A.
\[ V_{out} = \left(1 + \frac{R_2}{R_1}\right)V_{in} - \frac{R_2}{R_1}V_{ref} \]
NOISE GAIN = \(1 + \frac{R_2}{R_1}\)

B.
\[ V_{out} = -\frac{R_2}{R_1}V_{in} - \frac{R_2}{R_3}V_{ref} \]
NOISE GAIN = \(1 + \frac{R_2}{R_1 \parallel R_3}\)

C.
\[ V_{out} = -\frac{R_2}{R_1}V_{in} + \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right)V_{ref} \]
NOISE GAIN = \(1 + \frac{R_2}{R_1}\)
Many industrial applications still require ADCs that can handle ±10V signals. This can be solved with the AD8475 and AD8476 ‘Funnel Amplifiers’.
Single-Ended Level Shifter with Gain Requires Rail-to-Rail Op Amp

- **NOISE GAIN** = \( 1 + \frac{R_2}{R_1} = 5 \)
- **SIGNAL GAIN** = \( -\frac{R_2}{R_1} = -4 \)

**INPUT COMMON-MODE VOLTAGE** = +0.3V

\[ V_{CM} = V_1 \left[ 1 + \frac{R_2}{R_1} \right] = +1.5V \]

**OUTPUT SWING** = +1.5V –/+ 1V

**INPUT RANGE** = +0.5V TO +2.5V

**OUTPUT SWING REQUIRED** = 5
Differential Amplifier Drivers for ADCs
Typical Single-Ended (A) and Differential (B) Input Transients of CMOS Switched Capacitor ADC

- Differential charge transient is symmetrical around mid-scale and dominated by linear component
- Common-mode transients cancel with equal source impedance

Note: Data Taken with 50Ω Source Resistances
Advantages of Differential Analog Input Interfaces for Data Converters

- Differential inputs give **twice the signal** swing vs. single-ended (Especially important for low voltage single-supply operation)
- Differential inputs help suppress **even order distortion** products
- Many IF/RF **components** such as SAW filters and mixers are differential
- Differential inputs suppress **common mode ADC switching noise** including LO feed-through from mixer and filter stages
- Differential ADC designs allow better internal component matching and tracking than single-ended. Less need for trimming

- If you drive them single-ended, you will have degradation in distortion and noise performance
- However, many signal sources are single-ended, so the differential amplifier is useful as a single-ended to differential converter
Positioning the Noise Reduction Filter to Reduce the Effects of the Op Amp Noise

(A) Positioning the Noise Reduction Filter to Reduce the Effects of the Op Amp Noise

- Amp noise integrated over amp BW or ADC BW, whichever is less

(B) Amp noise integrated over filter noise bandwidth only

- ADCs typically have very high input bandwidths, usually much greater than \( f_s/2 \)
- Low distortion drive amplifiers typically have high bandwidths
- Placing a simple LPF or BPF placed between the AMP and the ADC is an excellent noise reduction technique
- The output capacitor of the filter absorbs some of the ADC input transient currents.
### Relationship Between Equivalent Noise Bandwidth and 3-dB Bandwidth for Butterworth Filter

<table>
<thead>
<tr>
<th>NUMBER OF POLES</th>
<th>EQ. NOISE BW / 3dB BW</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.57</td>
</tr>
<tr>
<td>2</td>
<td>1.11</td>
</tr>
<tr>
<td>3</td>
<td>1.05</td>
</tr>
<tr>
<td>4</td>
<td>1.03</td>
</tr>
<tr>
<td>5</td>
<td>1.02</td>
</tr>
</tbody>
</table>

![Diagram illustrating the relationship between equivalent noise bandwidth and 3-dB bandwidth for Butterworth filters. The diagram shows the decrease in dB with increasing frequency (f), highlighting the 3-dB point and the equivalent noise bandwidth (EQ.NOISE BW).]
ADA4940-1 Driving AD7986 18-Bit PulSAR® ADC in +5V Application

- $V_{\text{REF}} = +4.096V$
- $V_{\text{IN}} = \pm 2.048V$
- $V_{\text{CM}} = +2.048V$
- $V_{\text{OCM}}$

**Components:**
- ADR4544
- AD7986, 2MSPS
- AD7982, 1MSPS
- AD7984, 1.33MSPS
- 18-BIT PulSAR ADC

**Specifications:**
- SNR = 98dB
- For AD7982 Serial Output

**Notes:**
- After filter, noise = 7µV rms due to amp
- Signal = 8.192V p-p differential
- SNR = 118dB @ ADC input

**Diagram Details:**
- **Input Range:** 8.192V p-p Diff.
- **LPF Cutoff:** 1MHz

**Mathematical Expressions:**
- $V_{\text{CM}} = +2.048V$
- $V_{\text{OCM}}$
- $+2.048V +/\ - 2.048V$
- $+2.048V -/\ + 2.048V$
- $3.9nV/\sqrt{Hz}$
AD813x, ADA493x and ADL556x Differential ADC Drivers Functional Diagram

(EQUIVALENT CIRCUIT:

\[
\text{GAIN} = \frac{R_F}{R_G}
\]
DC Coupled ADA4930-1 Driving AD9629
12-Bit 20-80MSPS CMOS ADC, Baseband signal

AD9629 SPECS:
INPUT BW = 700MHz
1 LSB = 488µV
SNR = 71.2dB

AD4930 OUTPUT NOISE = 1.2nV/√Hz x √1.57×32×10^6 = 8.5µV rms

OUTPUT SNR = 20 log 0.707/8.5×10^-6 = 98dB
AD8475: Differential Funnel Amplifier + ADC Driver

Large Input Signal

Low Voltage ADC Inputs
**AD8475 : Funnel Amplifier + ADC Driver**

- Interface ±10V or ±5V signal on a single-supply amplifier
- Integrate 4 Steps in 1
  - Attenuate
  - Single-Ended-to-Differential Conversion
  - Level-Shift
  - Drive ADC
- Drive differential 18-bit SAR ADC up to 4MSPS with few external components

![AD8475 Circuit Diagram](image)
ADC Dynamic Performance Measurement
Important AC Performance Specifications for ADCs

- Signal-to-Noise and Distortion Ratio (SINAD)
- Effective Number of Bits (ENOB)
- Signal-to-Noise Ratio (SNR)
- Single and Multitone Spurious Free Dynamic Range (SFDR)
- Total Harmonic Distortion (THD)
- Second Order Intermodulation Distortion (IMD2)
- Third Order Intermodulation Distortion (IMD3)
- Input Bandwidth (Small and full power BW)
- ACLR

Must Also Remember These:
- Minimum Sampling Frequency
- Pipeline Delay (Latency)
- Settling time and overvoltage recovery
Ideal N-bit ADC Quantization Noise

\[
\text{RMS VALUE} = \frac{q}{\sqrt{12}}
\]

\begin{align*}
\text{ERROR} & \quad (\text{INPUT} - \text{OUTPUT}) \\
\text{DIGITAL OUTPUT} & \quad \uparrow \\
\text{ANALOG INPUT} & \quad \downarrow \\
\end{align*}
Quantization Noise Spectrum

RMS VALUE = \( \frac{q}{\sqrt{12}} \)  \( q = 1 \) LSB

MEASURED OVER DC TO \( \frac{f_s}{2} \)

NOISE SPECTRAL DENSITY

\( \frac{q}{\sqrt{12}} \) \( \sqrt{\frac{f_s}{2}} \)

SNR = 6.02N + 1.76dB + 10\log_{10} \left( \frac{f_s}{2 \cdot BW} \right) \) FOR FS SINEWAVE

Process Gain
Effect of Input-Referred Noise on ADC "Grounded Input" Histogram

P-P INPUT NOISE

≈ 6.6 × RMS NOISE

NUMBER OF OCCURRENCES

STANDARD DEVIATION

= RMS NOISE (LSBs)
SINAD, ENOB, SNR, and THD

◆ SINAD (Signal-to-Noise-and-Distortion Ratio):
  ● The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics and noise, but excluding DC.

◆ ENOB (Effective Number of Bits):

\[
ENOB = \frac{SINAD - 1.76\text{dB}}{6.02\text{dB}}
\]

◆ SNR (Signal-to-Noise Ratio, or Signal-to-Noise Ratio Without Harmonics):
  ● The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, excluding the first 5 harmonics and DC

◆ THD (Total Harmonic Distortion):
  ● The ratio of the rms signal amplitude to the mean value of the root-sum-square of its harmonics (generally only the first 5 harmonics are significant) and excluding DC
AD9244 14-Bit, 65MSPS ADC
SINAD and ENOB for 1V and 2V Input Span

NOTE: AD9244 Full Power Input Bandwidth = 750MHz
Relationship Between SINAD, SNR, and THD

- \( \text{SNR} = 20 \log \frac{S}{N} \)
- \( \text{THD} = 20 \log \frac{S}{D} \)
- \( \text{SINAD} = 20 \log \frac{S}{N + D} \)

- \( \text{SINAD} = -10 \log \left( 10^{-\text{SNR}/10} + 10^{-\text{THD}/10} \right) \)

- SNR, THD, and SINAD must be measured using the same signal amplitude.
- SINAD = THD + N if the measurement bandwidth is the same.
- Typically only the first 5 harmonics are included in the distortion term, D
Relationship Between SNR, Sampling Clock Jitter, Quantization Noise, DNL, and Input Noise

\[
\text{SNR} = -20 \log_{10} \left( (2\pi \times f_a \times t_{\text{j rms}})^2 + \frac{2}{3} \left( \frac{1 + \varepsilon}{2^N} \right)^2 + \frac{2 \times \sqrt{2} \times V_{\text{NOISErms}}}{2^N} \right)^{1/2}
\]

- \( f_a \) = Analog input frequency of fullscale input sinewave
- \( t_{\text{j rms}} \) = Combined rms jitter of internal ADC and external clock
- \( \varepsilon \) = Average DNL of the ADC (typically 0.41 LSB for AD6645)
- \( N \) = Number of bits in the ADC
- \( V_{\text{NOISErms}} \) = Effective input noise of ADC (typically 0.9LSB rms for AD6645)

If \( t_j = 0, \varepsilon = 0, \) and \( V_{\text{NOISErms}} = 0 \), the above equation reduces to the familiar:

\[
\text{SNR} = 6.02 N + 1.76 \text{dB}
\]
Dynamic Performance Analysis of ADCs Using FFT Techniques

ANALOG INPUT
Fin

ADC Under Test

FIFO

M-Point FFT Processing

Spectral Output

Fs

N
Ideal 12-Bit ADC, Input = 2.111MHz, \( f_s = 82\text{MSPS} \), Average of 5 FFTs, \( M = 16,384 \)

ADC FULLSCALE

SNR = 6.02N + 1.76dB = 74dB

FFT NOISE FLOOR = 113dB

RMS QUANTIZATION NOISE LEVEL

PROCESSING GAIN = \( 10 \log \frac{M}{2} = 39\text{dB} \)

Data Generated Using ADIsimADC®

\[ N = 12, M = 16,384 \quad \text{Bin Spacing} = \frac{f_s}{M} \]
AD9643 14-Bit ADC, \( f_{\text{in}} = 128.048 \text{MHz} \), \( f_s = 210 \text{MSPS} \), \( M = 65,536 \) (SuperNyquist)

\[ N = 14, \quad M = 65,536 \quad \text{Bin Spacing} = \frac{f_s}{M} \]
Location of Distortion Products: Input Signal = 7MHz, Sampling Rate = 20MSPS

HARMONICS AT: $|\pm Kf_s \pm nf_a|$
n = ORDER OF HARMONIC, $K = 0, 1, 2, 3, \ldots$

$K = 0, 1, 2, 3, \ldots$
Spurious Free Dynamic Range (SFDR) in Communications Systems

SINGLE TONE SFDR

MULTITONE SFDR

WORST SPUR

FREQUENCY

SIGNAL LEVEL dB

FS

SFDR (dBc)

SFDR (dBFS)

FREQUENCY

WORST SPUR

FS

SFDR (dBc)

SFDR (dBFS)
### Tradeoffs: SNR, SFDR, and Bandwidth Versus Power Consumption

<table>
<thead>
<tr>
<th></th>
<th>System</th>
<th>Power</th>
<th>SNR</th>
<th>SFDR</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Per Ch</td>
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<td></td>
</tr>
<tr>
<td>AD9446, 16 bits</td>
<td>2.3 W</td>
<td>79 dB</td>
<td>90 dBFs</td>
<td>540 MHz</td>
<td></td>
</tr>
<tr>
<td>100 MSPS</td>
<td>(CMOS outputs)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD9262, 16 bits</td>
<td>0.3 W</td>
<td>&gt;83.0 dB</td>
<td>89 dBFs</td>
<td>10 MHz</td>
<td></td>
</tr>
<tr>
<td>130 MSPS</td>
<td>(Dual)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD9650, 16 bits</td>
<td>0.325 W</td>
<td>80.0 dB</td>
<td>92 dBFs</td>
<td>500 MHz</td>
<td></td>
</tr>
<tr>
<td>105 MSPS</td>
<td>Dual (1.8V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD9643, 14 bits</td>
<td>0.395 W</td>
<td>71.9 dB</td>
<td>90 dBFs</td>
<td>650 MHz</td>
<td></td>
</tr>
<tr>
<td>250 MSPS</td>
<td>(1.8V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD9467, 16 bits</td>
<td>1.3 W</td>
<td>76.2 dB</td>
<td>95 dBFs</td>
<td>900 MHz</td>
<td></td>
</tr>
<tr>
<td>250 MSPS</td>
<td>(1.8V)</td>
<td>75 dB (210 MHz)</td>
<td>93 dBFs (210 MHz)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SNR, SFDR, and Bandwidth Tradeoffs for Simplified Sample-and-Hold Hold Model

**SMALLER $C_H$:**
- Higher Bandwidth
- Higher Noise (Lower SNR)
- Less Load on A1, Lower Distortion (Higher SFDR)
- Min Sampling Rate

**Larger $C_H$:**
- Lower Bandwidth
- Lower Noise (Higher SNR)
- More Load on A1, Higher Distortion (Lower SFDR)
High Speed ADC in Digital Receivers
Generic IF Sampling Wideband Software Radio Receiver and Transmitter

- **RF**
- **RECEIVER**
  - **BPF**
  - **LNA**
  - **MIXER**
  - **IF**
  - **BPF**
  - **ADC**
  - **RSP, DSP**
  - **CHANNELS**

- **RF**
- **TRANSMITTER**
  - **BPF**
  - **PA**
  - **MIXER**
  - **IF**
  - **BPF**
  - **DAC**
  - **TSP, DSP**
  - **CHANNELS**
Undersampling and Frequency Translation Between Nyquist Zones

ZONE 1

ZONE 2

ZONE 3
Undersampling and Oversampling Combined Results in Process Gain

\[ \text{SNR} = 6.02N + 1.76\text{dB} + 10\log_{10} \left( \frac{f_s}{2\cdot BW} \right) \]

\text{FOR FS SINEWAVE}