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Processors and IP from Cortus

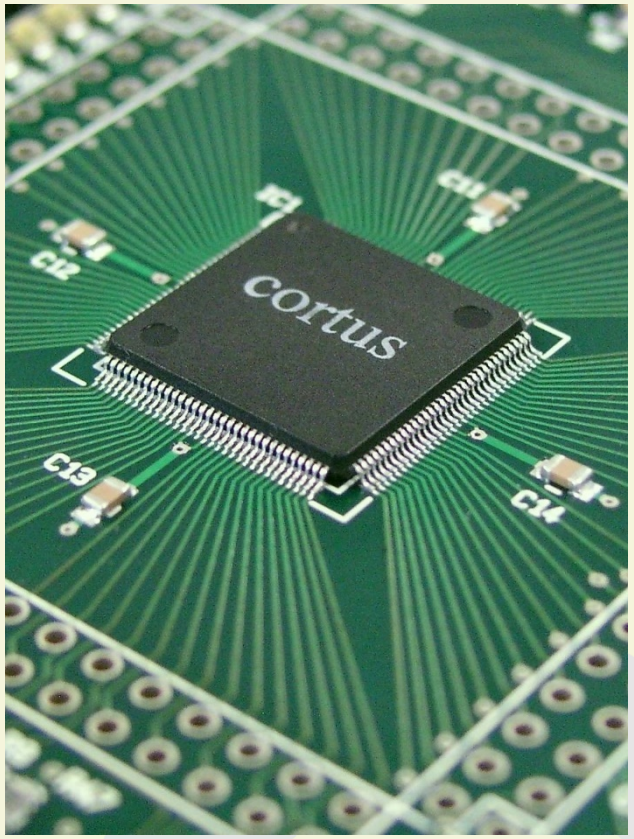
Technologies and Solutions for Embedded Systems

David Kerr-Munslow, Product Manager

The smart choice!

Overview

- About Cortus
- Embedded Systems
- Processor Architecture
- Processors
- Applications
- Questions



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Cortus at a Glance

- Founded in 2005
- Independent, European company
- Closed first VC funding round July 2013
- Focused on developing more power- and silicon-efficient 32-bit processors
- Proven foundation for security
- Offices in France, Germany, Korea, UK & USA

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Embedded Systems

- Based around SoC
  - Processor
  - Peripherals
  - Analogue Functions (PHYs etc)
  - Memory
    - RAM
    - ROM/Flash/EEPROM

Characteristics of Embedded Systems

- Flexibility and diversity
- Power consumption
- Ubiquity
  - Cost
    - Die size
    - Battery size
    - Component count
  - Size
- Apt for real time

Why 32 bits?

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- Software is getting bigger
  - Protocol stacks
  - System features
  - User interfaces
- > 64 KBytes
- C
  - `sizeof(int *) == sizeof(int)`

Memory Bandwidth

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- Registers are faster
- Registers can be dual port
- Flash is “slow”
- RAM is not quick
- Load / Store architecture

Instruction Length

- Diadic or triadic instructions
- Conditional instructions
- Number of registers
  - Bits to specify register
- Instruction bus width
- Complexity of fetch logic

Why 16 registers?

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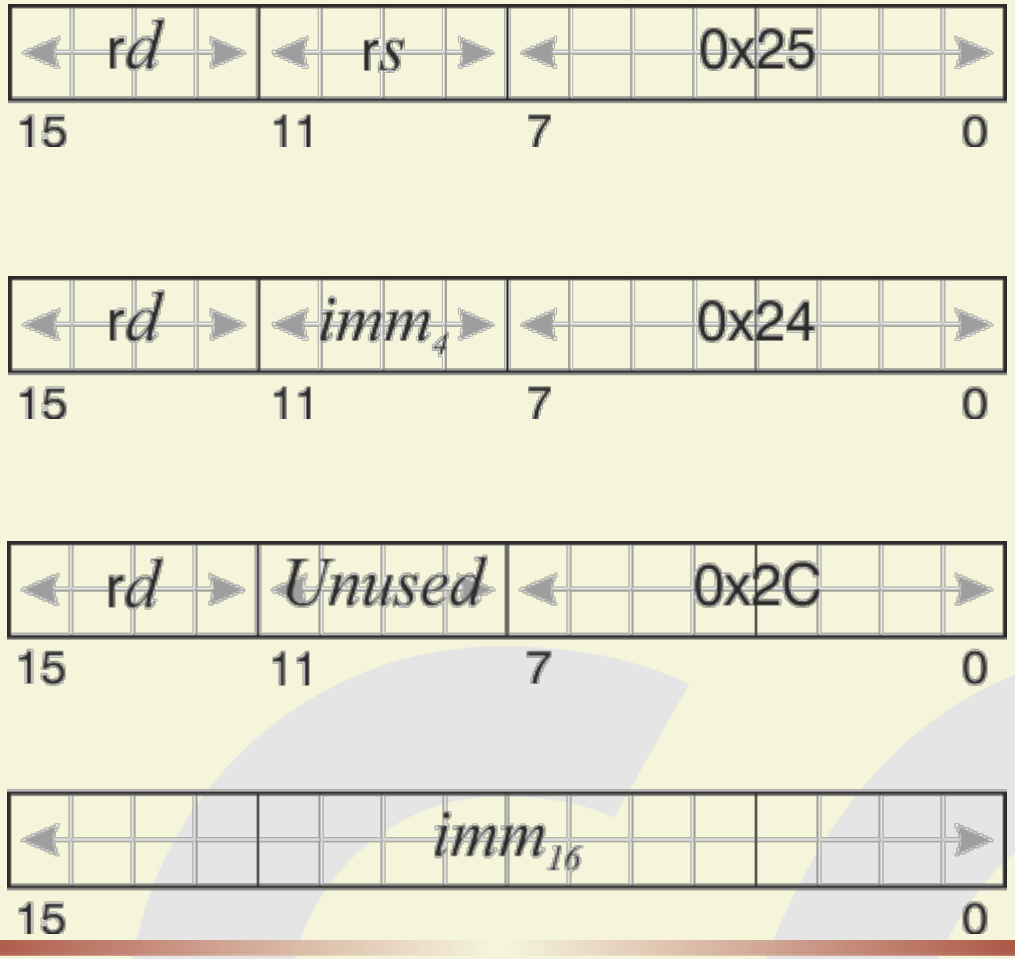
- SPARC 32 visible registers
  - … of 160
- MIPS 31 registers
- Alpha 32 registers
- AVR 32 registers
- x86 6 registers (16 now)
- VAX 16 registers, 12 general purpose

v1 Instructions



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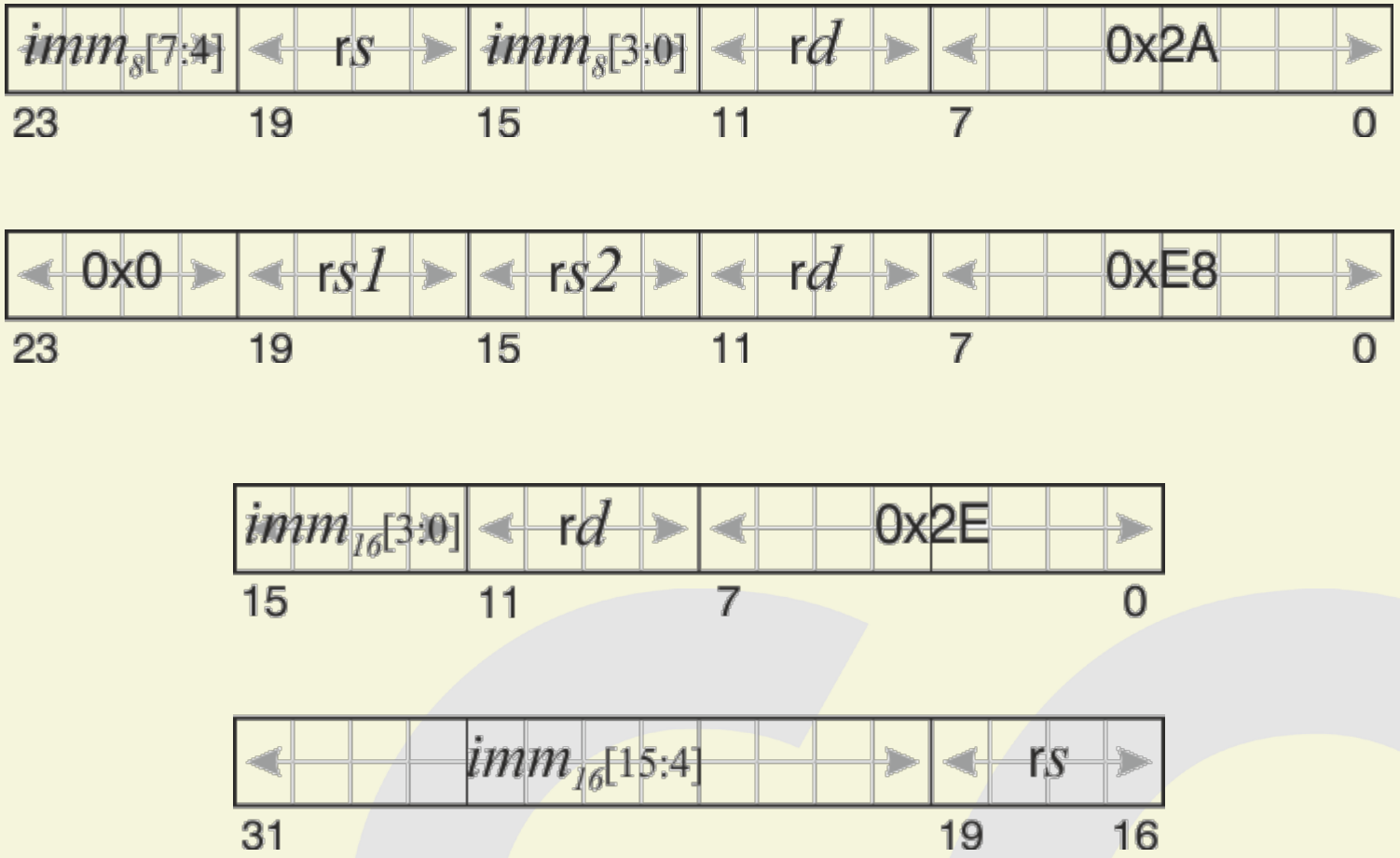
Code Density

- Number of instructions required to implement a given functionality
- Influences
  - Code size
  - Number of instruction fetches
  - Effectiveness of cache

New v2 Instructions



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Pipeline Stages

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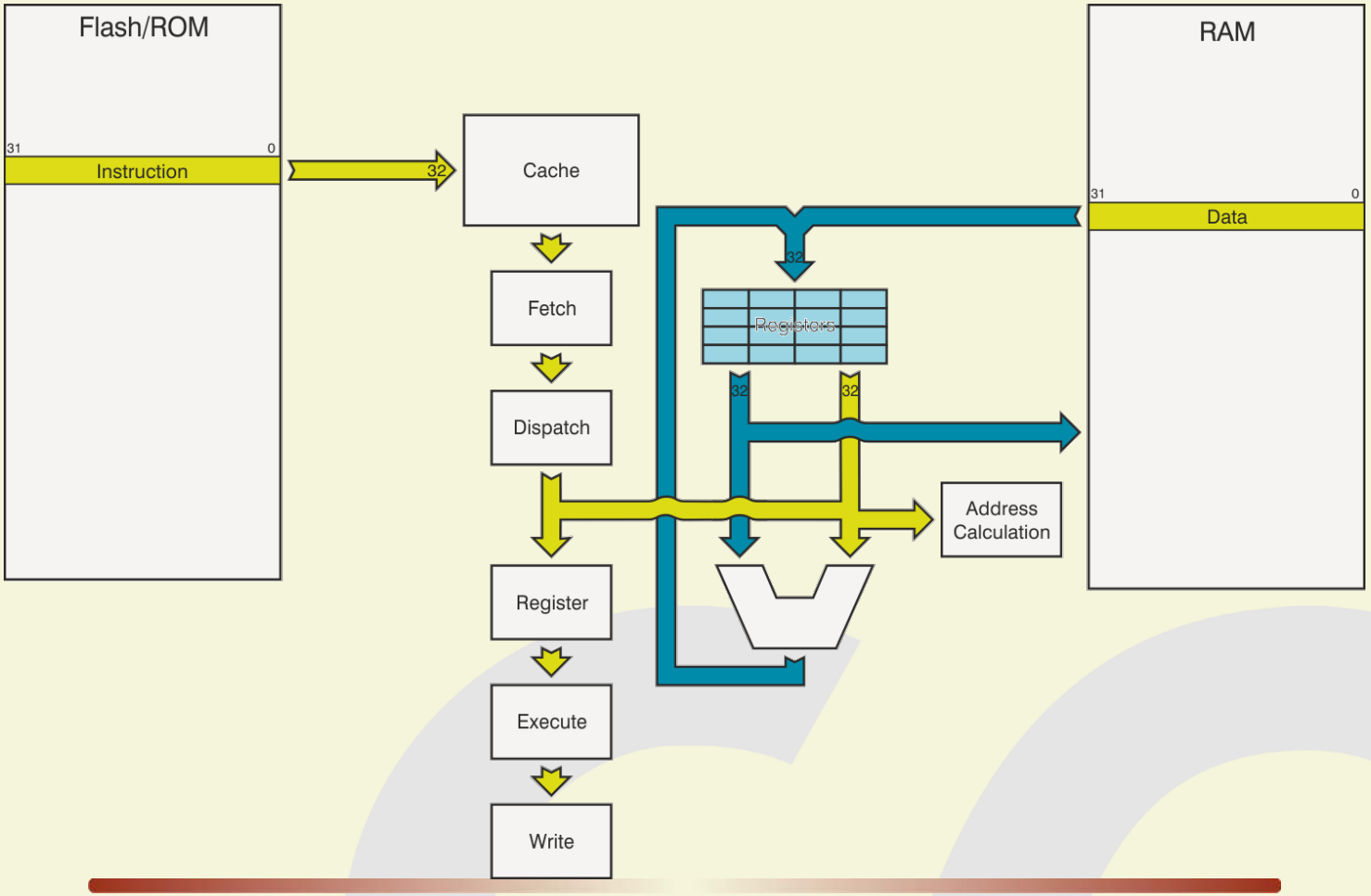
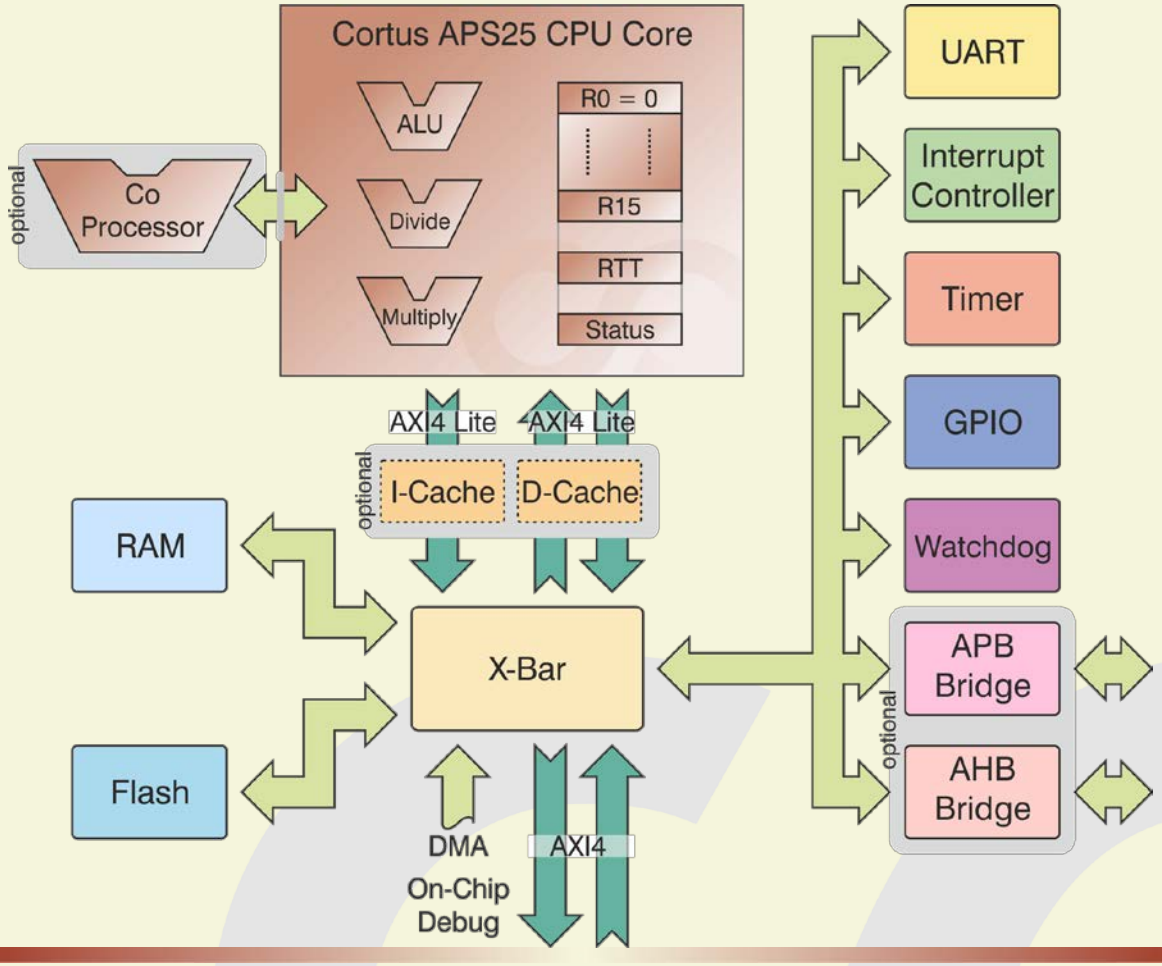
- More
  - Higher clock frequency
  - Greater branch/interrupt cost
- Fewer
  - Lower power
  - Lower silicon footprint

Basic Architecture



In a System



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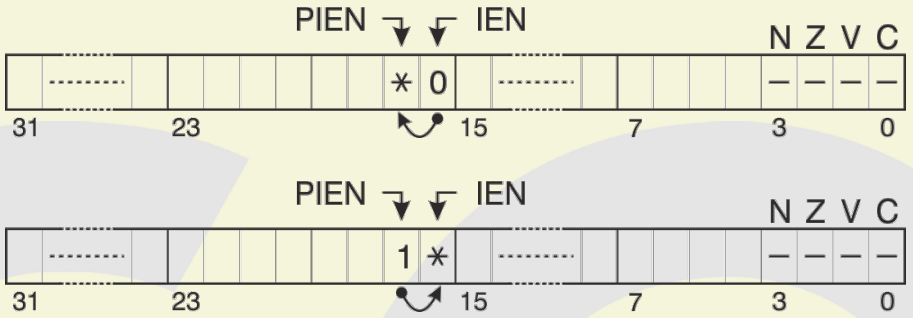
Interrupts

- Vectored interrupts
- Trap instruction
- RTT register
- PSR, interrupt enable



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What's Missing?

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- Branch prediction
- Speculative execution
- Virtual memory
  - Re-execution of instructions

Cortus Processors

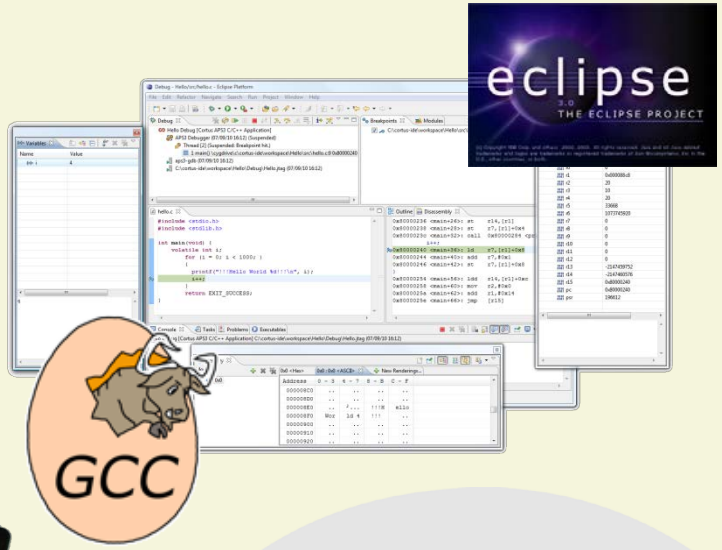
- v1 instruction set
  - APS1
  - APS3R
  - APS5
  - FPS6
- v2 instruction set
  - APS23
  - APS25

Common Characteristics

- Modern RISC
- Load / store architecture
- 16 registers
  - R0 always 0
  - R15 link register
  - R1 stack pointer (by convention)

Compiler & Tools

- Ported at same time as design
- Tools are essential
- IDE
- Debugging



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Peripherals

- Design peripherals for 32 bit system
  - One register per function
  - Registers word aligned
  - Avoid need for bit manipulation
- Compare Intel 8259A

Applications

- Over 750 million devices
- Wireless
  - Remote metering
- Smart cards
- SIM cards
- Security solutions

Thank-you!

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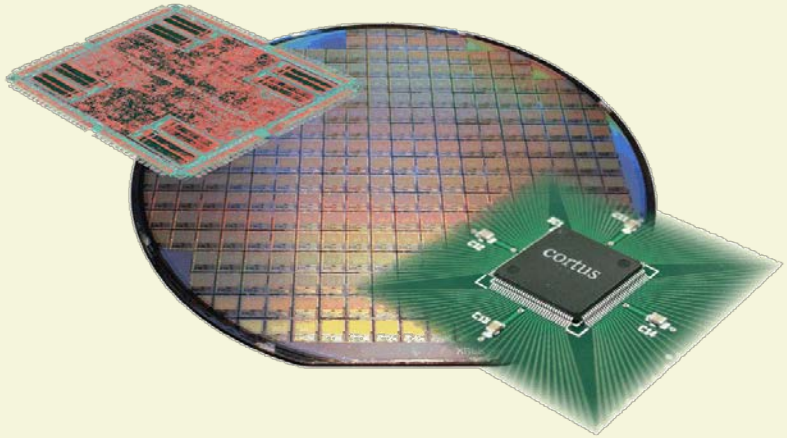

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