

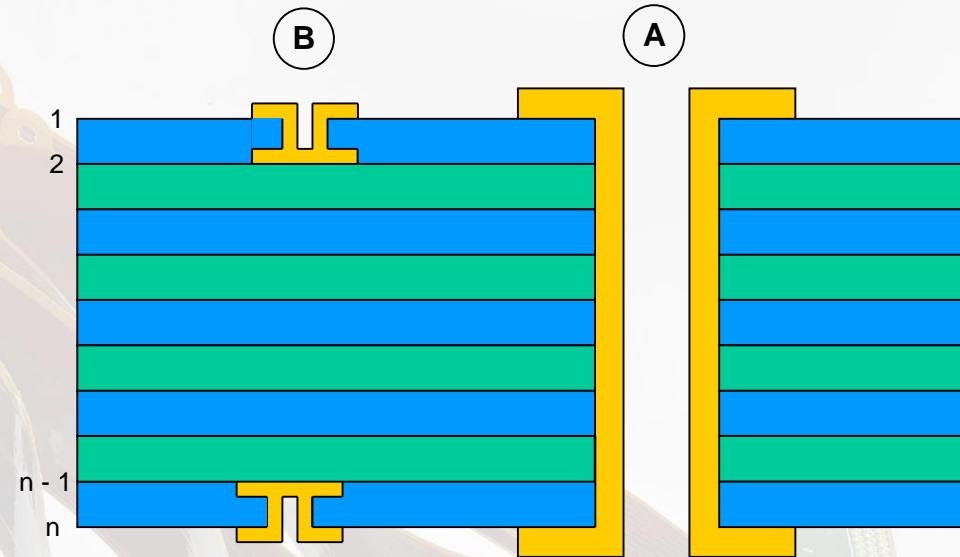
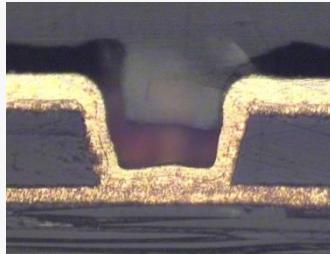
- les ratios de perçage.
- Matière low CTE.
- Epargne de vernis autour des vias.
- Problèmes pour demain.

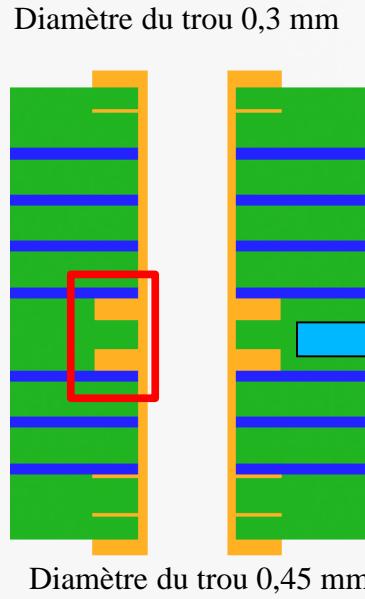
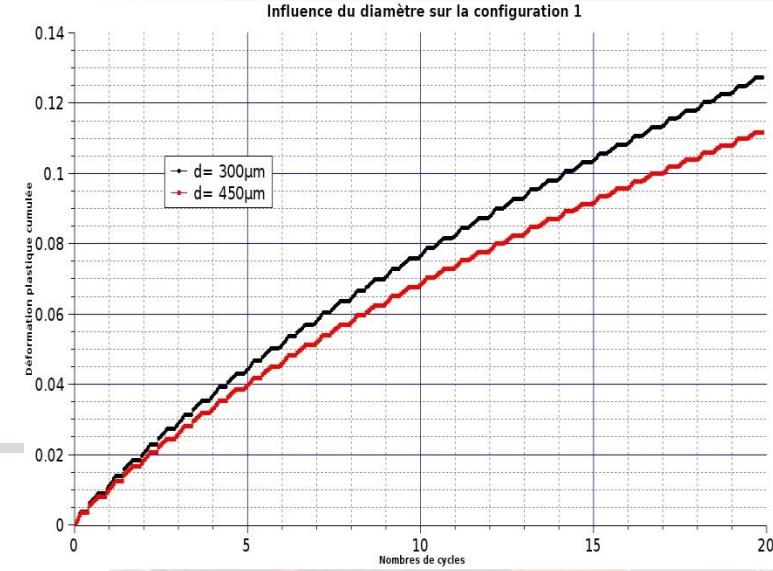
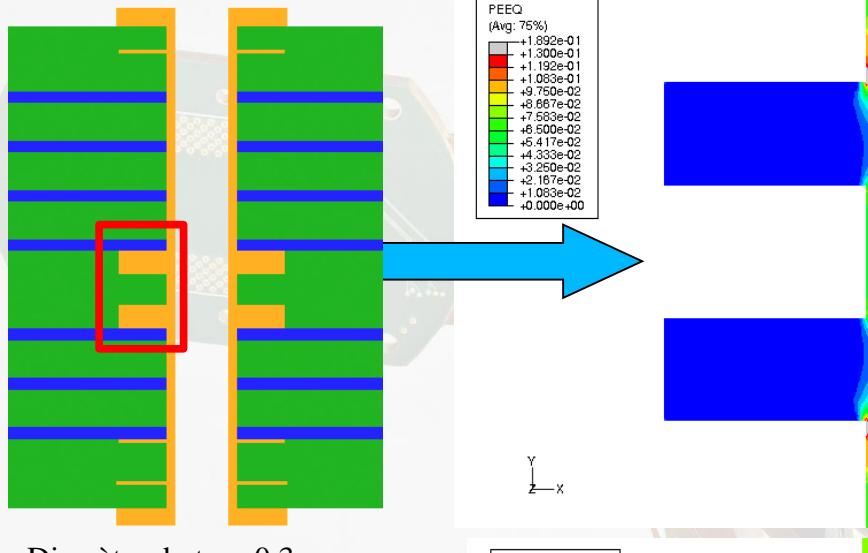


Les ratios de perçage à respecter:

A/ Trous traversants:
 Ép. / diam. ≤ 8

B/ μ vias:
 Ép. / diam. $\leq 0,8$

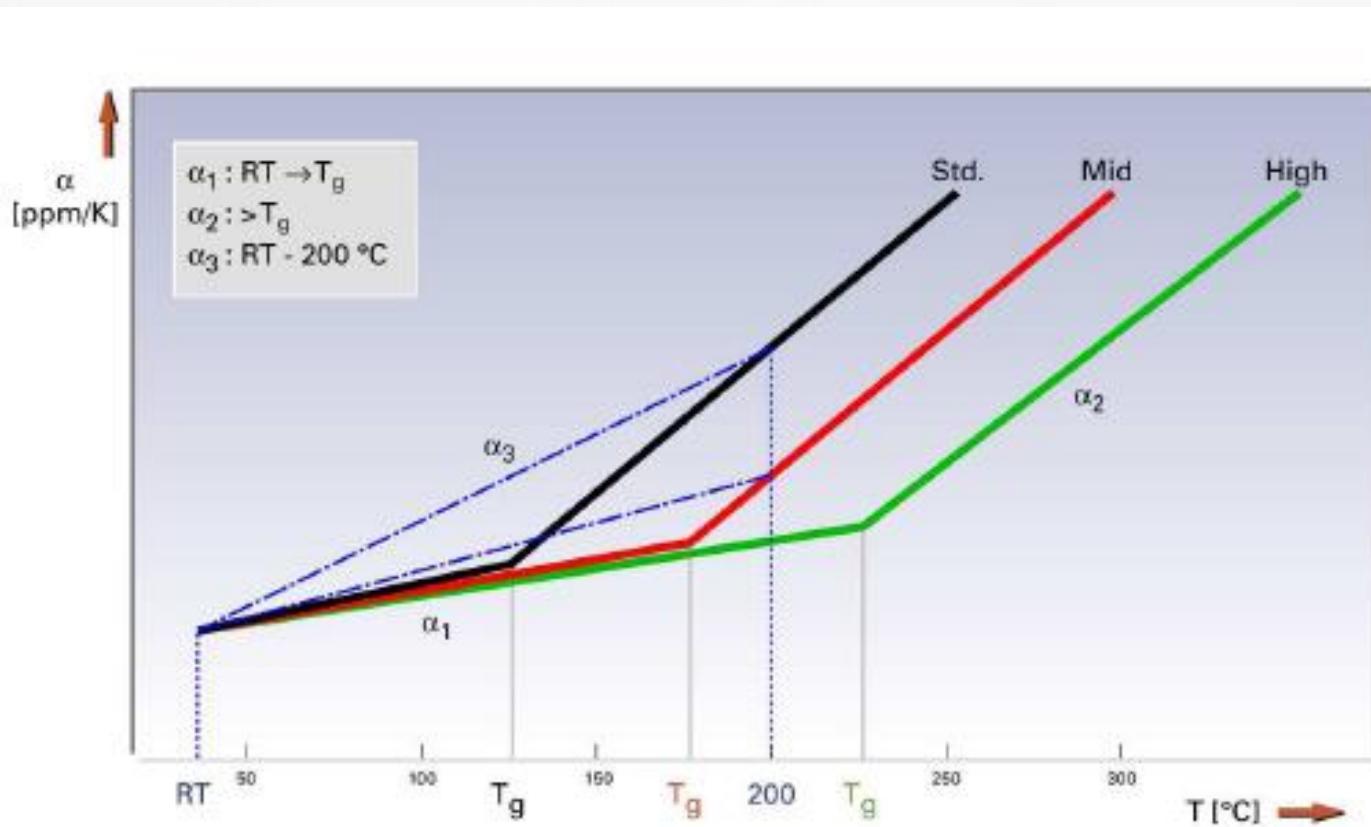




Estimation des durées de vie:

	$\varnothing 0,3 \text{ mm}$	$\varnothing 0,45 \text{ mm}$
Nombre de cycles à rupture (N) (coef)	N	$N \times 1.3$

- μ via très fiables



Minimiser les contraintes en z:

-matériaux chargés

-haut T_g



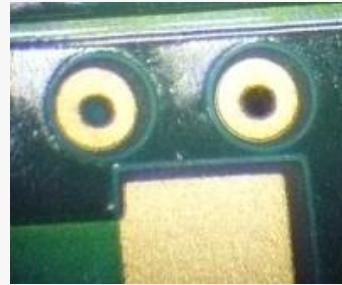
Epargnes de vernis autour des vias 1/2



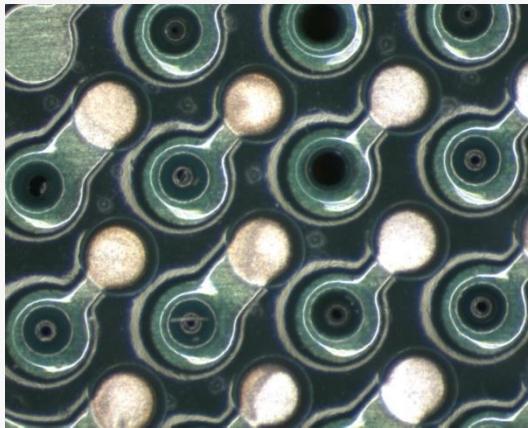
Protection de la piste, risque de court circuit avec le plan d'alimentation



Risque de déséquilibre du composant en cas de fluage de l'aliage dans le via



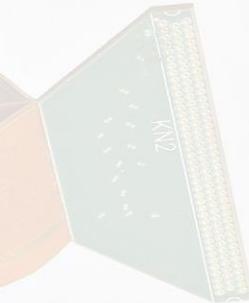
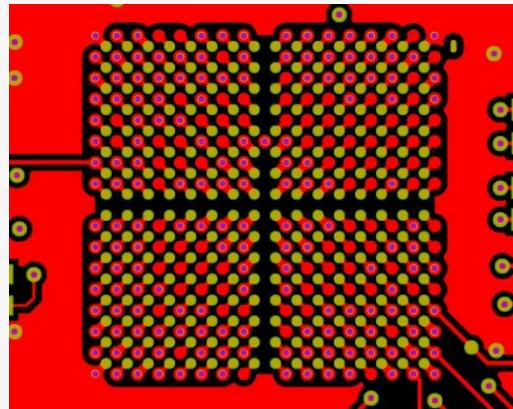
Risque de court circuit entre via et plage CMS



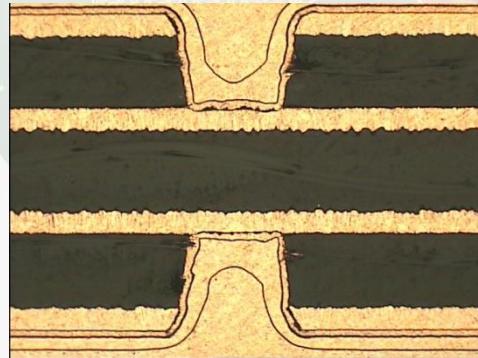
**Vias bouchés. Risque de pollution
et d'oxydation du via**

**La solution: utilisation de point de centre couplé au
dépôt du vernis au spray.**

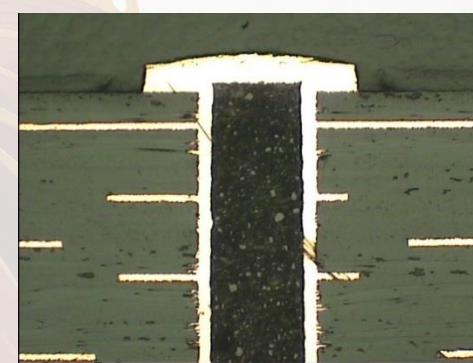
Diam. Point de centre = Diam. Via + 100µm



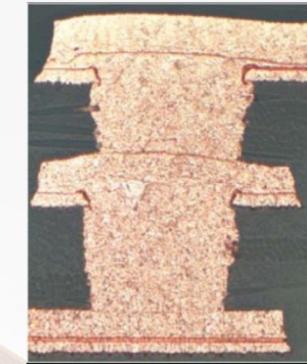
μ via fill-in pour via
in pad



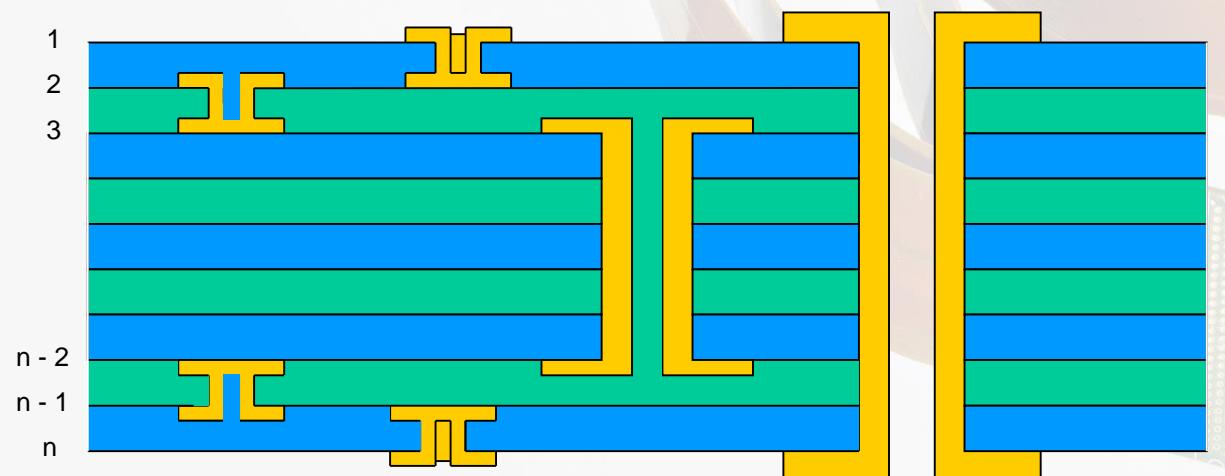
Pad on hole



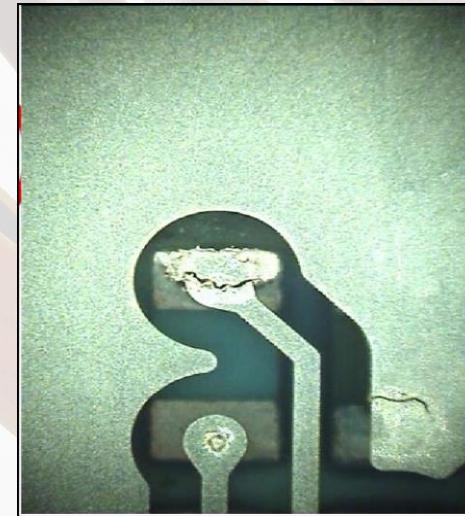
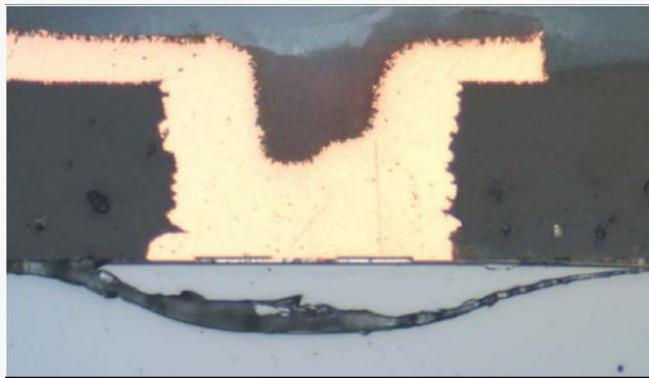
Vias stackés



multicouches séquentiel μ via HDI (2 – n – 2)



- Utiliser des matériaux avec des CTE x,y proches de la céramique (5 ppm)
- Tenue des plages de cuivre
- Avoir des composants enterrés
- ...





Le niveau de performance attendu et la complexification des designs rend la relation concepteur-fabricant indispensable:

La solution:

Co-design

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